

## INTERNATIONAL SEARCH REPORT

Inte  nal Application No  
PCT/IB2004/004226A. CLASSIFICATION OF SUBJECT MATTER  
IPC 7 G06T1/20 G06F9/46

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06T G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category <sup>a</sup>	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	-/-	

 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

## \* Special categories of cited documents :

- \*A\* document defining the general state of the art which is not considered to be of particular relevance
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Date of the actual completion of the international search

Date of mailing of the international search report

24 February 2005

04/03/2005

Name and mailing address of the ISA

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PCT/IB2004/004226	

## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>BECKER J ET AL: "Automatic parallelism exploitation for FPL-based accelerators" SYSTEM SCIENCES, 1998., PROCEEDINGS OF THE THIRTY-FIRST HAWAII INTERNATIONAL CONFERENCE ON KOHALA COAST, HI, USA 6-9 JAN. 1998, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, vol. 7, 6 January 1998 (1998-01-06), pages 169-178, XP010262779 ISBN: 0-8186-8255-8</p> <p>section "3. Parallelism Exploitation by Partitioning Compilation Techniques"</p> <p>section "3.1 Profiling-driven Host/Accelerator Partitioning for Exploiting Task Level Parallelism"</p> <p>figures 4,6</p> <p>section "3.2 Resource-driven Partitioning for Exploiting Statement Level Parallelism"</p> <p>-----</p>	1,2,4, 7-11
A	<p>NICOLESCU C ET AL: "A data and task parallel image processing environment" PARALLEL COMPUTING, ELSEVIER PUBLISHERS, AMSTERDAM, NL, vol. 28, no. 7-8, August 2002 (2002-08), pages 945-965, XP004375029</p> <p>ISSN: 0167-8191</p> <p>abstract</p> <p>section "3.2. Data parallelism of low-level image operators"</p> <p>figures 1-3</p> <p>section "4. The task parallel framework"</p> <p>section "4.1. The image application task graph model"</p> <p>-----</p>	1-11
A	<p>FRESSE V ET AL: "ARIAL: rapid prototyping for mixed and parallel platforms" PARALLEL COMPUTING, ELSEVIER PUBLISHERS, AMSTERDAM, NL, vol. 28, no. 7-8, August 2002 (2002-08), pages 1179-1202, XP004375039</p> <p>ISSN: 0167-8191</p> <p>abstract</p> <p>section "2. The global prototyping process"</p> <p>figures 1,2</p> <p>section "3.1.1. Using SynDEX in the implementation"</p> <p>section *4.3. The automatic translator"</p> <p>-----</p>	1-11

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>IONESCU F ED - INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "Mapping image rendering operations onto parallel processors"</p> <p>1996 INTERNATIONAL SEMICONDUCTOR CONFERENCE. SINAIA, ROMANIA, OCT. 9 - 12, 1996, INTERNATIONAL SEMICONDUCTOR CONFERENCE, NEW YORK, IEEE, US, vol. VOL. 2 CONF. 19, 9 October 1996 (1996-10-09), pages 167-170, XP010200550 ISBN: 0-7803-3223-7</p> <p>title</p> <p>summary</p> <p>section "2. Partitioning and mapping of the data domain and of the program"</p> <p>section "3. Striped partitioning"</p> <p>-----</p>	1-11